

METHOD OF ETCHING A LATERAL TRENCH UNDER A DRAIN JUNCTION OF A MOS TRANSISTOR

Field of the Invention

5 The invention relates to MOS transistor. In particular, it relates to a MOS transistor with reduced drain capacitance.

Background of the Invention

 A typical MOS transistor, as indicated by reference numeral 100 in
10 Figure 1, includes a drain region 102, and a source region 104, formed in a substrate 106, and separated by a channel region 108. A metal gate 110 serves as the controlling electrode. For ease of description, the metal contacts to the drain region 102 and source region 104, have not been shown, but would serve to provide electrical contact with the drain and source regions, in a manner commonly known in the art. It
15 will be appreciated that the drain 102 is oppositely doped to the substrate 106 and that a reverse biased p-n junction exists between the drain region 102 and substrate 106, which accounts for a substantial amount of drain capacitance.

 It will be appreciated that this parasitic capacitance has a significant effect on f_{Max} (the maximum frequency at which the device can practically be operated) and f_T
20 (the cut-off frequency where voltage gain is unity). It would therefore be desirable to be able to increase f_{Max} and f_T for high speed applications.

Summary of the Invention

 The present invention proposes a MOS transistor with reduced drain
25 capacitance comprising a drain and a source formed in a substrate, at least one vertical trench for lateral isolation, and a lateral trench extending at least partly under the drain, which may be filled with air or an insulator. The vertical trench requires a $\langle 110 \rangle$ sidewall orientation in a $\langle 100 \rangle$ silicon wafer.

 For purposes of this application, drain and source are used interchangeably
30 with the terms drain region and source region. Also, the term substrate is used

generically for any material in which the drain and source are formed, whether or not that is a well or the underlying substrate.

Further, according to the invention, there is provided a method of forming a laterally extending trench underneath the drain of a MOS transistor, comprising
5 making use of the natural crystal orientation for the semiconductor material in which the BJT is formed and accordingly choosing a predetermined crystal configuration, and using an anisotropic etchant to etch the trench. The semiconductor material may be silicon and the crystal configuration is preferably a standard $\langle 100 \rangle$ configuration. The laterally extending trench therefore preferably has an orientation of $\langle 110 \rangle$. The
10 etchant is preferably a wet anisotropic silicon etchant such as KOH, typically with alcohol such as ethanol, and water. It may also be another type of wet anisotropic etchant such as TMAH.

Brief Description of the Drawings

15 Figure 1 is a section through a typical MOS transistor in an integrated circuit, Figure 2 is a section through a one embodiment of a MOS transistor of the invention,
Figures 3 –5 show three crystal orientations,
Figure 6 shows a typical isotropic etch profile,
20 Figure 7 shows a typical anisotropic etch profile in a $\langle 100 \rangle$ direction,
Figure 8 shows a typical anisotropic etch profile in a $\langle 110 \rangle$ direction, and
Figures 9 –16 show the steps of forming a laterally extending isolation trench in accordance with one embodiment of the invention.

25 Detailed Description of the Invention

It has been determined that by providing an isolation region between the extrinsic base and the collector of a BJT, the base-collector parasitic capacitance can be improved to achieve an improved f_{Max} and f_T for the BJT device. In order to achieve this, one approach adopted by the applicants as part of the present invention is
30 to etch a laterally extending trench underneath the drain, which extends at least

partially under the drain. One such embodiment is illustrated in Figure 2 which shows a MOS transistor 200 having a drain 202 and a source 204 formed in a substrate 206, and separated by a channel region 208 under a gate 210. In addition vertically extending shallow trench isolation regions (STIs) 212, 214 are formed next to the drain 202 and source 204, respectively as shown. In accordance with the invention a lateral trench 220 is formed underneath the drain 202, extending from the vertical STI 212 to act as an isolation region underneath the drain 202 and thereby reduce the drain capacitance. In the present embodiment the lateral trench 220 extends entirely underneath the drain 202 and even somewhat past the drain region 220. It will be appreciated that other embodiments may have the lateral trench extending only partially underneath the drain thereby only partially limiting the drain capacitance.

Another aspect of the invention relates to the manner in which the laterally extending isolation regions, such as the trench 220 in Figure 2 are formed. The present invention makes use of the natural crystal orientation of the semiconductor material in which the transistor is formed, and a specific etchant type to achieve the desired configuration of the laterally extending trench underneath the drain.

Crystals, such as silicon crystals, have a particular configuration that is determined by the way the atoms in the crystal are aligned. For ease of reference, terminology has evolved to define three basic configurations: $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$. These are best understood with reference to Figures 3, 4 and 5, respectively. This is discussed in more detail in "Physics of Semiconductor Devices" by S. M. Sze (see in particular on page 10), which is incorporated by reference herein. Typically BJTs are formed in silicon wafers that are grown to have a crystal orientation of $\langle 111 \rangle$ for the top surface. In contrast MOS and BiCMOS devices are typically formed in $\langle 100 \rangle$ orientation wafers (in the case of BiCMOS SiGe is typically used). The present invention proposes using a $\langle 100 \rangle$ silicon wafer (top surface having a $\langle 100 \rangle$ crystal orientation) and forming the laterally extending isolation trenches between the extrinsic base regions and collector in a $\langle 110 \rangle$ direction. By doing this in conjunction with an anisotropic etch process, the desired isolation trench, such as the trench 220 was found to be achievable. In particular, in one embodiment, an anisotropic wet etch

using KOH with alcohol and water was found to work well. In this embodiment ethanol was used for the alcohol. In another embodiment TMAH was used as the wet anisotropic etchant.

Figure 6 shows the typical etch profile for isotropic etchants. As can be seen, 5 etching the silicon 600 through a window 602 results in substantially similar etching in the vertical and the lateral directions. Figure 7 contrasts this with the use of a wet anisotropic etchant such as KOH with alcohol and water when etching through a window 702 in a silicon wafer 700 having a $\langle 100 \rangle$ crystal orientation. This provides an etch profile where the trench has an angle of 54.74° as shown in Figure 7. 10 However, when combining the wet anisotropic etchant with a crystal orientation $\langle 110 \rangle$ a trench with very steep vertical sides and negligible lateral etching is achieved as shown in Figure 8. Figure 8 shows a deep, narrow trench 800 formed in a silicon wafer 802 having a $\langle 110 \rangle$ orientation.

Using this concept, the present invention makes use of a $\langle 100 \rangle$ orientation 15 wafer, thereby having the $\langle 110 \rangle$ crystal orientation in both the lateral and vertical directions with respect to the wafer flat or notch. Thus, the rectangular mask opening, used to form the vertical trench is formed such that its rectangular opening, in the plane of the wafer, is oriented similarly, either perpendicular or parallel to the wafer flat or notch. This allows deep lateral trenches to be etched using a wet anisotropic 20 etchant. Preferably a plasma/dry etch is used for etching the vertical trench.

The process of forming one embodiment of a MOS transistor of the invention will now be discussed in more detail with respect to Figures 9-16.

Figure 9 shows a silicon substrate 900 having a $\langle 100 \rangle$ orientation. A shallow trench 902 is etched into this substrate using, standard techniques for forming a 25 shallow trench isolation (STI) region. As will become clearer below, the trench 902, will ultimately serve to form the STI regions 212 next to the drain.

An organic fill material 1000 such as BCB, polyamide, Perspex, etc, is then deposited on the silicon 900 to fill the trench 902, as shown in Figure 10.

As shown in Figure 11, the organic fill 1000 is then etched back to leave an organic fill plug 1100 in the bottom of the trench 902. Preferably an oxygen based plasma is used for etching back the organic fill.

5 A plasma enhanced TEOS (PETEOS) 1200 is then deposited as shown in figure 12, whereafter the excess PETEOS is etched away, leaving a spacer sidewall, as shown in Figure 13. In this embodiment a reactive ion etch (RIE) was used to etch away the excess PETEOS to leave the PETEOS spacer 1300.

Thereafter, more of the organic fill plug 1100 is etched away using, for example, O₂ plasma or wet etch. This is shown in Figure 14, and leaves a short lateral
10 undercut under the PETEOS spacer 1300.

Thereafter, the laterally extending trench 1500 is etched in the <110> direction by making use of an anisotropic wet etch such as KOH with ethanol and water, or TMAH, etc. This is shown in Figure 15. The one side of the trench 1500 will serve to form an isolation trench under one MOS transistor, such as the trench 220, while the
15 other side of the trench 1500 will be used to form a lateral isolation trench for an adjacent MOS structure. It will be appreciated that, in such a case the drains of the two adjacent transistors will be separated by the STI that will be formed in the trench 902, e.g. the STI 212 in Figure 2. Even though Figure 2 shows only the one transistor, it will be appreciated that the other transistor would extend to the left hand side of the
20 transistor 200.

Thereafter, the rest of the organic fill plug is removed, e.g., using an oxygen plasma and cleaning with sulphuric acid or peroxide and followed by dilute HCL or peroxide. Thereafter, the resultant vertical trench is filled with insulating material such as PETEOS or other high step coverable insulating material, to define a STI
25 region 1600 as shown in Figure 16. It will be appreciated that if the vertical trench has a less aggressive aspect ratio, other insulating material with less step coverage can be used instead of PETEOS. The STI region 1600 is similar to the region 212 of the Figure 2 embodiment. In this embodiment, however, the laterally extending trench 1500 is not filled with insulating material as in the Figure 2 embodiment but remains
30 as an air gap that will exist underneath the drain that will subsequently be formed. As

noted above, the trench 1500 extends on either side of the STI region 1600 in Figure 16. It will be appreciated that each of these two trenches (indicated as 1510 and 1512) will ultimately extend under a drain of a transistor (the drains being formed in the silicon material 900 in any standard way known in the art).

5 It will also be appreciated that while the present invention was described with respect to some specific embodiments, different embodiments may be adopted without departing from the scope of the invention as defined by the claims.

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